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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,755	04/09/2004	Masanao Yokoyama	8019-1039	8776

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,755	YOKOYAMA, MASANAO	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,17,18 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-11,13 and 14* is/are rejected.

7)☒ Claim(s) *6,7,12,17,18,20-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/820,755 filed 04/09/2004 and amendment filed 10/17/2006.

2. Claims 1-14, 17, 18, 20-23 are pending in the Application. Claims 15, 16, 19 have been cancelled from the Application. Claims 21-23 have been added to the Application.

3. Applicant's arguments have been fully considered but they are partly persuasive.

Claim Objections

4. Claims 6, 7, 10, 12, 17, 18, 20-23 are objected to because of the following informalities:

Claim 6 line 3 after "passing" delete "therethrough" insert –through inside of said hard-macro--

Claim 10 line 2 replace "plurality" with --pluralities--

Claim 12 line 3 after "passing" delete "therethrough" insert –through inside of said hard-macro--

Claim 17 line 9 after "through" insert –inside--

Claim 23 line 7 after "through" insert –inside of--

It has to be noted that proposed amendment to the claims is based on the Specification of the instant Application on the Page 10 (line 17).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi (US Patent 5,331,572).

With respect to claim 1 Takahashi teaches a first hard-macro arranged on a semiconductor chip and constituting a part of a semiconductor integrated circuit that includes plural blocks and plural hard-macros other than the first hard-macro that are connected to each other with signal wires (as shown on the Fig. 17 input/output block 37 arranged in the corner of the semiconductor chip (col. 1, ll.36-37), wherein plurality of macro-blocks is arranged in the integrated circuit layout and macro-blocks are wired/connected with signal wires (col. 1, ll.25-29, Fig. 16)), including at least one signal wire passing through the first hard-macro, wherein the at least one signal wire is formed in the first hard-macro before the first hard-macro is arranged on the semiconductor chip (within power supply wiring patterns 41 included in the input-output block 37 as shown on the Fig. 19 (43-45)), and the wire starts at a first outer edge of the first hard-macro and terminates at a second outer edge of the first hard-macro intersecting with the first outer edge (as shown on the Fig. 19 the wiring pattern 41 passing through input-output block 37 starting at one outer edge of the block 37 (input) and ending in the other outer edge of the block 37 (output) (col. 1, ll.46-47)).

With respect to claims 2-5, 8-11 Takahashi teaches:

Claims 2: wherein the first and second outer edges are adjacent to each other (as shown on the Fig. 19 the wiring pattern arranged on the block 37 such as input on one outer edge and the output on the adjacent outer edge);

Claim 3: wherein the first and second outer edges are perpendicular to each other (as shown on the Fig. 19);

Claim 4: wherein the at least one signal wire is L-shaped (as shown on the Fig. 19 wiring pattern 41 is arranged on the block 37 in L-shape);

Claim 5: wherein the at least one signal wire is linear (as shown on the Fig. 19 wiring pattern 41 is arranged on the block 37 by linear wires);

Claim 8: further including a repeater inserted in the at least one signal wire (within inserting buffer including wiring pattern 40 as shown on the Fig. 18, wherein wiring pattern 40 connected to the wiring pattern 41 (col. 1, ll.42-44));

Claim 9: wherein the hard-macro includes a plurality of the at least one signal wires passing therethrough (within wiring pattern 41 as shown on the Fig. 19 passing through input/output/ block 37, wherein wiring pattern includes plurality of wires);

Claim 10: wherein the pluralities of signal wires are equally spaced away from adjacent ones (as shown on the Fig. 19)

Claim 11: wherein at least one of the plurality of signal wires includes a repeater inserted therein wire within inserting buffer including wiring pattern 40 as shown on the Fig. 18, wherein wiring pattern 40 connected to the wiring pattern 41 (col. 1, ll.42-44).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi as applied to claim 1 above, and further in view of Kaneko (US Patent Application Publication 20010025364).

With respect to claim 13 and 14 Takahashi teaches the limitations from which the claims depend. However Takahashi lacks the specifics regarding the type of hard-macros arranged on the chip layout. Kaneko teaches:

Claim 13: wherein the first hard-macro is a random access memory (RAM) (as shown on the Fig. 2 depicting typical arrangement macro cells on the semiconductor chip 200, wherein one of the plurality of macro cells is RAM 203 (paragraph [0006]));

Claim 14: wherein the first hard-macro is a phase locked loop (PLL) (as shown on the Fig. 2 depicting typical arrangement macro cells on the semiconductor chip 200, wherein one of the plurality of macro cells is PLL 205 (paragraph [0006])). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Kaneko to teach the specifics subject matter Bednar does not teach, because the standard cell (chip) constructed by interconnecting plurality of macros, wherein one of the macros is PLL (abstract; paragraph [0038]).

Allowable Subject Matter

9. Claims 6, 7, 12, 17, 18, 20-23 have allowable subject matter and will be allowed after their amendment to overcome aforementioned objection of the claims 6, 12, 17 and 23.

Remarks

10. In the remarks Applicant argues in substance:

a) Takashi does not disclose a "signal wire" passing through the hard-macro as claimed in amended claim 1

b) As described in the specification at page 3, lines 14-19 the problem to be solved by the present invention is a detour wire relative to a path which "starts at a first outer edge of the hard-macro and terminates at a second outer edge of the hard-macro intersecting with the first outer edge".

11. Examiner respectfully disagrees for the following reasons:

With respect to a) Takashi discloses wiring pattern/signal wires 41 passing through macrocell 37 as shown on the Fig. 19.

With respect to b) it has to be noted that passage about "a detour wire relative to a path ..." was not found on the page 3, lines 14-19 of the instant specification. Moreover, even if this passage was there, this statement is irrelevant, since it's not in the claim 1 of the instant Application.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helen Rossoshek
Examiner
Art Unit 2825

PAUL DINH
PRIMARY EXAMINER